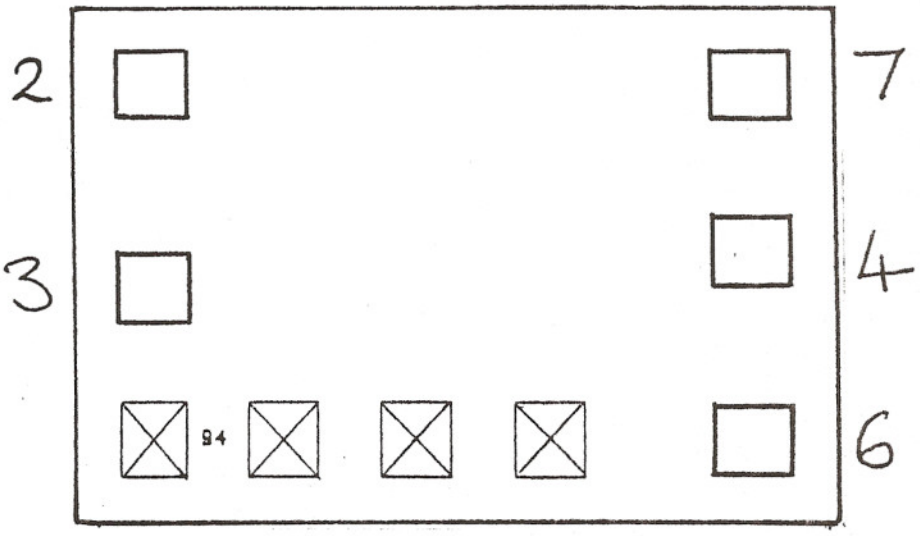
ISO9001:2000 Certified SCI Quality System

Sierra Components, Inc.

2222 Park Place Building 3 Suite E • Minden, Nevada 89423
Phone: 775.783.4940 Fax: 775.783.4947

Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Pad	Function
1	NC
2	V_{inv}
3	$V_{non-inv}$
4	$-V_{CC}$
5	NC
6	V_{out}
7	$+V_{CC}$
8	NC

NOTE: The chip back may be connected to $-V_{CC}$ or left floating.

Topside Metal: Au
Backside: Si
Backside Potential: -Vcc
Mask Ref: 94
Bond Pads (Mils): 4 x 4

APPROVED BY: **DIE SIZE (Mils): 44 x 31** **DATE: 3/16/00**
MFG: National **THICKNESS: 14** **P/N: CLC404**